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EXAMINER	
MAI, TAN V	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/826,527	Applicant(s) LANGHAMMER, MARTIN	
	Examiner Tan V Mai	Art Unit 2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6-25-01, 7-23-01 & 1-22-02*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5-6*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The abstract of the disclosure is objected to because the Abstract contains the undefined acronym "DSP". All such acronyms should be defined at the instance of their first use within the Abstract. Correction is required. See MPEP § 608.01(b).

2. Claims 7-10, 18-21 and 26-34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per dependent claim 7, the term "**analysis** logic" is not understood. Is "**analysis** logic" a type of Boolean logic? Similarly noted claim 18 and claim 26 (**analysis** circuit).

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-3 and 11-17 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Fandrianto et al.

As per independent claim 1, Fandrianto et al disclose, e.g., see Fig. 4 and col. 2, lines 51-65, a **programmable** processor circuit comprising a multiplier-accumulators (148) and an arithmetic logic unit (154). The arithmetic logic unit is **programmable** reconfigurable for either a pixel mode or a word mode. Each of multiplier-accumulators, e.g., see Fig. 13, has a **programmable** "overflow clamp" (626). Therefore, Fandrianto et al teach the claimed combination.

As per dependent claim 2, Fandrianto et al disclose the claimed "**rounding**" feature, e.g., see col. 21, lines 27-46.

As per dependent claim 3, Fandrianto et al disclose the claimed "**saturation**" [equivalent term "clamping"] feature, e.g., see col. 21, lines 27-46.

Due to the similarity of independent claim 11 to claim 1, it is rejected under a similar rationale.

As per dependent claim 12, Fandrianto et al disclose the claimed feature because the arithmetic logic unit (154) does not include a word conditioning logic "multiplier-accumulators (148)".

As per dependent claim 13, Fandrianto et al disclose the claimed feature because the arithmetic logic unit (154) does have feed back path via other elements.

As per dependent claim 14, Fandrianto et al disclose the claimed feature because the arithmetic logic unit (154) and word conditioning logic "multiplier-accumulators (148)" have interconnection via other elements.

Due to the similarity of dependent claim 15 to claims 2-3, it is rejected under a similar rationale.

As per dependent claims 16-17, Fandrianto et al's system should have memory means for storing desired data.

5. Claims 1-3, 11-12 and 14-17 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Duncan et al.

As per independent claim 1, Duncan et al disclose, e.g., see Fig. 6A and col. 14, line 66 to col. 15, line 67 & col. 17, lines 30-51, a **programmable** arithmetic block comprising multipliers-adders and accumulator (680). The multipliers-adders have a **reconfiguration** register (682). The accumulator (680) also has a **programmable** feature "[t]he arithmetic block 450 also has **configuration options** for saturation arithmetic and rounding". Therefore, Duncan et al teach the claimed combination.

As per dependent claim 2, Duncan et al disclose the claimed **"rounding"** feature.

As per dependent claim 3, Duncan et al disclose the claimed **"saturation"** feature.

Due to the similarity of independent claim 11 to claim 1, it is rejected under a similar rationale.

As per dependent claim 12, Duncan et al disclose the claimed feature because the multipliers-adders do not include a word conditioning logic "accumulator".

As per dependent claim 14, Duncan et al disclose the claimed feature because the multipliers-adders coupled to the word conditioning logic "accumulators".

Due to the similarity of dependent claim 15 to claims 2-3, it is rejected under a similar rationale.

As per dependent claims 16-17, Duncan et al's system should have memory means for storing desired data.

6. Claims 1-3, 11-12 and 14-17 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Thi et al.

As per independent claim 1, Thi et al disclose, e.g., see Fig. 34 and paragraphs [0306]-[0309], a **programmable** multiply-accumulate data path comprising a "computation unit" (4030-4046) and a "word condition logic" (4048, 4052 & 4050). The "computation unit" (4030-4046) has **prgrammable** "pointer controllers" (4030-4034) and "word condition logic" (4048, 4052 & 4050) has a **programmable** shifter (4048). Therefore, Thi et al teach the claimed combination.

As per dependent claim 2, Thi et al disclose the claimed "**rounding**" feature.

As per dependent claim 3, Thi et al disclose the claimed "**saturation**" feature.

Due to the similarity of independent claim 11 to claim 1, it is rejected under a similar rationale.

As per dependent claim 12, Thi et al disclose the claimed feature because the "computation unit" (4030-4046) does not include word conditioning logic "accumulator".

As per dependent claim 14, Thi et al disclose the claimed feature because the "computation unit" (4030-4046) coupled to "word conditioning logic " (4048,4052 & 4050).

Due to the similarity of dependent claim 15 to claims 2-3, it is rejected under a similar rationale.

As per dependent claims 16-17, Thi et al's system should have memory means for storing desired data.

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 22-27 and 31-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fandrianto et al.

Fandrianto et al. have been discussed in paragraph #4 above.

As per dependent claims 22-25, the claims detail a digital processing / printed circuit board comprising the claimed "programmable logic circuit". It would have been obvious to a person having ordinary skill in the art at the time the invention was made to design the claimed invention according to Fandrianto et al's teachings because the "programmable logic circuit" can be built in a digital processing / printed circuit board as claimed.

Due to the similarity of dependent claims 31-34 to claims 22-25, they are rejected under a similar rationale.

As per claims 26-27, the claim adds the "data conditioning and **analysis** circuit" feature (lines 5-6). According to Applicant's specification, the "analysis circuit" is old and well known in the art. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to substitute Fandrianto et

al's the "rounding logic and saturation logic" by the claimed "data conditioning and **analysis** circuit" as claimed.

9. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fandrianto et al. in view of Lim et al.

Fandrianto et al. have been discussed in paragraph #4 above.

As per claim 4, the claim adds "rounding logic and saturation logic are arranged in series". Lim et al disclose the detail feature (e.g., see Abstract). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Lim et al's "rounding logic and saturation logic are arranged in series" in Fandrianto et al, thereby making the claimed invention, because the proposed device is a computing unit having "rounding logic and saturation logic are arranged in series" as claimed.

10. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fandrianto et al. in view of Lim et al as applied to claim 4 above, and further in view of Nguyen et al.

As per claim 5, the claim adds "monitoring the signals in the computing unit using the saturation unit" feature. Nguyen et al disclose (e.g., see Fig. 3) a saturation detection unit (304) is parallel with adder/select (302). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Nguyen et al's "saturation detection unit" in Fandrianto et al & Lim et al, thereby making the claimed invention, because the proposed device is a computing unit having

"rounding logic and saturation logic are arranged in series" & "monitoring the signals in the computing" features as claimed.

As per claim 6, Nguyen et al disclose the saturation detection unit (304) is parallel with adder/select (302).

11. Claims 22-27 and 31-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duncan et al.

Duncan et al. have been discussed in paragraph #5 above.

As per dependent claims 22-25, the claims detail a digital processing / printed circuit board comprising the claimed "programmable logic circuit". It would have been obvious to a person having ordinary skill in the art at the time the invention was made to design the claimed invention according to Duncan et al's teachings because the "programmable logic circuit" can be built in a digital processing / printed circuit board as claimed.

Due to the similarity of dependent claims 31-34 to claims 22-25, they are rejected under a similar rationale.

As per claims 26-27, the claim adds the "data conditioning and **analysis** circuit" feature (lines 5-6). According to Applicant's specification, the "analysis circuit" is old and well known in the art. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to substitute Duncan et al's the "rounding logic and saturation logic" by the claimed "data conditioning and **analysis** circuit" as claimed.

12. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Duncan et al. in view of Lim et al.

Duncan et al. have been discussed in paragraph #5 above.

As per claim 4, the claim adds "rounding logic and saturation logic are arranged in series". Lim et al disclose the detail feature (e.g., see Abstract). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Lim et al's "rounding logic and saturation logic are arranged in series" in Duncan et al, thereby making the claimed invention, because the proposed device is a computing unit having "rounding logic and saturation logic are arranged in series" as claimed.

13. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duncan et al. in view of Lim et al as applied to claim 4 above, and further in view of Nguyen et al.

As per claim 5, the claim adds "monitoring the signals in the computing unit using the saturation unit" feature. Nguyen et al disclose (e.g., see Fig. 3) a saturation detection unit (304) is parallel with adder/select (302). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Nguyen et al's "saturation detection unit" in Duncan et al & Lim et al, thereby making the claimed invention, because the proposed device is a computing unit having "rounding logic and saturation logic are arranged in series" & "monitoring the signals in the computing" features as claimed.

As per claim 6, Nguyen et al disclose the saturation detection unit (304) is parallel with adder/select (302).

14. Claims 22-27 and 31-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thi et al.

Thi et al. have been discussed in paragraph #6 above.

As per dependent claims 22-25, the claims detail a digital processing / printed circuit board comprising the claimed "programmable logic circuit". It would have been obvious to a person having ordinary skill in the art at the time the invention was made to design the claimed invention according to Thi et al's teachings because the "programmable logic circuit" can be built in a digital processing / printed circuit board as claimed.

Due to the similarity of dependent claims 31-34 to claims 22-25, they are rejected under a similar rationale.

As per claims 26-27, the claim adds the "data conditioning and **analysis** circuit" feature (lines 5-6). According to Applicant's specification, the "analysis circuit" is old and well known in the art. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to substituteThi et al's the "rounding logic and saturation logic" by the claimed "data conditioning and **analysis** circuit" as claimed.

15. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Thi et al. in view of Lim et al.

Thi et al. have been discussed in paragraph #6 above.

As per claim 4, the claim adds "rounding logic and saturation logic are arranged in series". Lim et al disclose the detail feature (e.g., see Abstract). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Lim et al's "rounding logic and saturation logic are arranged in series" in Thi et al, thereby making the claimed invention, because the proposed device is a computing unit having "rounding logic and saturation logic are arranged in series" as claimed.

16. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thi et al. in view of Lim et al as applied to claim 4 above, and further in view of Nguyen et al.

As per claim 5, the claim adds "monitoring the signals in the computing unit using the saturation unit" feature. Nguyen et al disclose (e.g., see Fig. 3) a saturation detection unit (304) is parallel with adder/select (302). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Nguyen et al's "saturation detection unit" in Thi et al & Lim et al, thereby making the claimed invention, because the proposed device is a computing unit having "rounding logic and saturation logic are arranged in series" & "monitoring the signals in the computing" features as claimed.

As per claim 6, Nguyen et al disclose the saturation detection unit (304) is parallel with adder/select (302).

17. Claims 7-10, 18-21 & 28-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Cited references are art of interest.

19. The following is an examiner's statement of reasons for allowance: the recorded references do NOT teach or suggest the programmable logic device further comprising "analysis logic" feature as recited in dependent claims 7-10, 18-21 & 28-30.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan V. Mai whose telephone number is (703) 305-9761. The examiner can normally be reached on Tue-Fri from 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki, can be reached on (703) 305-9662. The fax phone numbers for the organization where this application or proceeding is assigned are:

Official (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

TAN V. MAI
PRIMARY EXAMINER